WHAT IS CLAIMED IS:

1. A processor comprising:

a circuit configured to generate an indication of a default operand size; and

an execution core coupled to receive a first instruction, wherein the execution core is configured to override the default operand size with a second operand size responsive to the first instruction having an implicit stack pointer reference.

2. The processor as recited in claim 1 further comprising a segment register and a configuration register coupled to the circuit, wherein the segment register is configured to store a segment selector locating a segment descriptor which includes a first operating mode indication and a second operating mode indication, and wherein the configuration register is configured to store an indication, and wherein the circuit is configured to generate the indication of the default operand size responsive to the first operating mode indication, the second operating mode indication, and the indication in the configuration register.

3. The processor as recited in claim 2 wherein the default operand size is 32 bits.

4. The processor as recited in claim 3 wherein the circuit is further configured to generate an indication of a default address size responsive to the first operating mode indication, the second operating mode indication, and the indication in the configuration register, and wherein the default address size is greater than 32 bits.

5. The processor as recited in claim 3 wherein the second operand size is 64 bits.

6. The processor as recited in claim 1 wherein the execution core is configured to override the default operand size with the second operand size in an absence of an operand size override encoding for the first instruction.

7. The processor as recited in claim 1 wherein the execution core is coupled to receive a near branch instruction, and wherein the execution core is configured to override the default operand size for the near branch instruction with the second operand size.

8. A method comprising:

generating a default operand size for instructions; and

overriding the default operand size with a second operand size for a first instruction responsive to the first instruction having an implicit stack pointer reference.

9. The method as recited in claim 8 further comprising generating an operating mode responsive to a first operating mode indication in a segment descriptor and a second operating mode indication in the segment descriptor and further responsive to an indication in a configuration register, wherein the generating the default operand size is responsive to the generating the operating mode.

10. The method as recited in claim 9 wherein the default operand size is 32 bits.

11. The method as recited in claim 10 further comprising generating a default address size responsive to the generating the operating mode, wherein the default address size is greater than 32 bits.

12. The method as recited in claim 10 wherein the second operand size is 64 bits.

13. The method as recited in claim 8 wherein the overriding the default operand size with the second operand size is performed in an absence of an operand size override encoding for the first instruction.

14. The method as recited in claim 8 further comprising overriding the default operand size for a near branch instruction with the second operand size.

15. A processor comprising:

a circuit configured to generate an indication of a default operand size; and

an execution core coupled to receive a near branch instruction, wherein the execution core is configured to override the default operand size with a second operand size responsive to the near branch instruction.

16. The processor as recited in claim 15 further comprising a segment register and a configuration register coupled to the circuit, wherein the segment register is configured to store a segment selector locating a segment descriptor which includes a first operating mode indication and a second operating mode indication, and wherein the configuration register is configured to store an indication, and wherein the circuit is configured to generate the indication of the default operand size responsive to the first operating mode indication, the second operating mode indication, and the indication in the configuration register.

17. The processor as recited in claim 16 wherein the default operand size is 32 bits.

18. The processor as recited in claim 17 wherein the circuit is further configured to generate an indication of a default address size responsive to the first operating mode

indication, the second operating mode indication, and the indication in the configuration register, and wherein the default address size is greater than 32 bits.

19. The processor as recited in claim 17 wherein the second operand size is 64 bits.

20. The processor as recited in claim 15 wherein the execution core is configured to override the default operand size with the second operand size in an absence of an operand size override encoding for the near branch instruction.

21. A method comprising:

generating a default operand size for instructions; and

overriding the default operand size with a second operand size for a near branch instruction.

22. The method as recited in claim 21 further comprising generating an operating mode responsive to a first operating mode indication in a segment descriptor and a second operating mode indication in the segment descriptor and further responsive to an indication in a configuration register, wherein the generating the default operand size is responsive to the generating the operating mode.

23. The method as recited in claim 22 wherein the default operand size is 32 bits.

24. The method as recited in claim 23 further comprising generating a default address size responsive to the generating the operating mode, wherein the default address size is greater than 32 bits.

25. The method as recited in claim 23 wherein the second operand size is 64 bits.

26. The method as recited in claim 21 wherein the overriding the default operand size with the second operand size is performed in an absence of an operand size override encoding for the near branch instruction.

5